

## Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

- 1 1. (currently amended) A circuit comprising:
  - 2 a first phase-locked loop (PLL) to receive a first reference signal and a first
  - 3 feedback signal, and to produce a data clock signal having a first frequency based at
  - 4 least in part upon ~~differences between~~ the first reference signal and a first feedback
  - 5 signal; and
  - 6 a second phase-locked loop PLL coupled to the first PLL phase-locked loop by a
  - 7 first signal path, the second phase-locked loop to receive a second reference signal on
  - 8 the first signal path and a second feedback signal on a second signal path, and to
  - 9 produce a second clock signal having a second frequency based at least in part upon
  - 10 ~~differences between~~ the second reference signal and the second feedback signal, the
  - 11 first feedback signal and the second reference signal being derived from the data clock
  - 12 signal and the second feedback signal being derived from the second clock signal,
  - 13 wherein the second reference signal and the second feedback signal have equivalent
  - 14 signal distribution delays.
- 1 2. (currently amended) The circuit of claim 1, further comprising a first divide-by-N
- 2 circuit coupled to the first PLL phase-locked loop circuit to divide the first frequency of
- 3 the data clock signal by a first integer value N to produce the first feedback signal
- 4 having a third frequency.
- 1 3. (currently amended) The circuit of claim 2, further comprising a divide-by-M
- 2 circuit coupled between the first PLL phase-locked loop circuit and the second PLL
- 3 phase-locked loop circuit to divide the first frequency of the data clock signal by an
- 4 integer value M to produce the second reference signal.

1 4. (original) The circuit of claim 3, wherein the divide-by-M circuit is equipped to  
2 divide the first frequency of the data clock signal by a selected one of a factor of 4, 2  
3 and 1.

1 5. (original) The circuit of claim 4, wherein the first divide-by-N circuit comprises a  
2 divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

1 6. (currently amended) The circuit of claim 3, further comprising a second divide-  
2 by-N circuit coupled to the second PLL-phase-locked loop to divide the second  
3 frequency of the second clock signal by a second integer value N to produce the  
4 second feedback signal, wherein the second integer value N is selected from a group of  
5 integer values including a low integer value, and a high integer value that is less than  
6 two times the low integer value.

1 7. (canceled)

1 8. (currently amended) The circuit of claim 1, wherein further comprising:  
2 the a-first signal path corresponding to the second reference signal; and  
3 the a-second signal path corresponding to the second feedback signal, wherein  
4 the first and second signal paths are equivalent in length.

1 9. (currently amended) A microprocessor-processor comprising:  
2 a processsing core;  
3 I/O-input-output circuitry; and  
4 a clock-generation circuit comprising:  
5 a first phase-locked loop (PLL) circuit coupled to the input-output circuitry by a  
6 first signal trace, the first phase-locked loop to produce-producing a first output signal  
7 having a first frequency based at least in part upon a first reference signal and a first  
8 feedback signal derived from the first output signal, and providing the first output signal  
9 to be used as a data clock signal for-to the I/O-input-output circuitry on the first signal  
10 trace; and

11           a second PLL circuitphase-locked loop coupled to the first PLL phase-locked  
12   loop by a second signal trace and to the processor core circuitry by a third signal trace,  
13   the second phase-locked loop to produce providing a second output clock signal to the  
14   processor core circuitry on the third signal trace, the second output signal having a  
15   second frequency based at least in part upon a second reference signal provided by the  
16   second signal trace and derived from the first output signal and a second feedback  
17   signal derived from the second output signal, ~~the second output signal to be used as a~~  
18   ~~clock signal for the processor core.~~

1   10. (currently amended) The microprocessor of claim 9, further comprising a first  
2   divide-by-N circuit coupled to the first PLL circuitphase-locked loop to divide the first  
3   frequency of the data clock signal by a first integer value N to produce the first feedback  
4   signal having a third frequency.

1   11. (currently amended) The microprocessor of claim 10, further comprising a  
2   divide-by-M circuit coupled between the first PLL circuitPhase-locked loop and the  
3   second PLL circuitPhase-locked loop to divide the first frequency of the data clock  
4   signal by an integer value M to produce the second reference signal.

1   12. (currently amended) The circuit processor of claim 11, wherein the divide-by-M  
2   circuit is equipped to divide the first frequency of the data clock signal by a selected one  
3   of a factor of 4, 2 and 1.

1   13. (currently amended) The circuit processor of claim 12, wherein the first divide-  
2   by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock  
3   signal by a factor of 4.

1   14. (currently amended) The circuit processor of claim 11, further comprising a  
2   second divide-by-N circuit coupled to the second PLL phase-locked loop to divide the  
3   second frequency of the core clock signal by a second integer value N to produce the  
4   second feedback signal, wherein the second integer value N is selected from a group of  
5   integer values including a low integer value and a high integer value that is less than  
6   two times the low integer value.

1 15. (canceled)

1 16. (currently amended) The ~~circuit~~ processor of claim 9, further comprising:  
2 a ~~first~~ signal ~~path~~ corresponding to the ~~second~~ reference ~~signal~~; and  
3 a ~~second~~ fourth signal trace ~~path~~ corresponding to provide the second feedback  
4 signal, wherein the ~~first~~ and ~~second~~ and fourth signal traces ~~paths~~ have equivalent  
5 signal distribution delays ~~are~~ equivalent in length.

1 17-19. (canceled)

1 20. (new) The processor of claim 16, wherein the second and fourth signal traces  
2 are equivalent in length.

**Amendments to the Drawings**

The attached sheet of drawings includes changes to Fig. 1. This sheet replaces the original sheet including Fig. 1. Figure 1 has been amended to include a "Prior Art" label.